WHAT IS CLAIMED IS:

1. A multi-protocol bus system, comprising:

a plurality of protocol indicators associated with an address space, each of said plurality of protocol indicators associated with a segment of said address space and configured to indicate a particular bus protocol; and

a bus protocol selection subsystem configured to employ control lines to implement one of said particular bus protocols in accordance with a selected one of said protocol indicators based upon an addressed segment of said address space.

2. The multi-protocol bus system as recited in Claim 1 further comprising a chip selection subsystem configured to provide a chip selection signal to an external device based upon said addressed segment of said address space.

3. The multi-protocol bus system as recited in Claim 2 wherein said external device is selected from the group consisting of:

a fast pattern processor,

a routing switch processor,

a Motorola-style bus architecture device, and

an Intel-style bus architecture device.

4. The multi-protocol bus system as recited in Claim 1 wherein said particular bus protocol is selected from the group consisting of:

a Motorola-style bus protocol, and

an Intel-style bus protocol.

5. The multi-protocol bus system as recited in Claim 1 wherein said control lines are selected from the group consisting of:

an address latch enable control line,

a chip select control line,

a read data strobe control line,

a write data strobe control line,

a ready control line,

a read/write select control line,

a data strobe control line, and

a data acknowledge control line.

6. The multi-protocol bus system as recited in Claim 1 wherein each segment of said address space is four kilobytes.

7. The multi-protocol bus system as recited in Claim 1 wherein said address space is a peripheral component interconnect (PCI) address space of thirty-two kilobytes.

8. A method of operating a multi-protocol bus system, comprising:

employing a plurality of protocol indicators associated with an address space, each of said plurality of protocol indicators associated with a segment of said address space and indicate a particular bus protocol; and

employing control lines to implement one of said particular bus protocols in accordance with a selected one of said protocol indicators based upon an addressed segment of said address space.

9. The method as recited in Claim 8 further comprising providing a chip selection signal to an external device with a chip selection subsystem based upon said addressed segment of said address space.

10. The method as recited in Claim 9 wherein said external device is selected from the group consisting of:

a fast pattern processor,

a routing switch processor,

a Motorola-style bus architecture device, and

an Intel-style bus architecture device.

11. The method as recited in Claim 8 wherein said particular bus protocol is selected from the group consisting of:

a Motorola-style bus protocol, and

an Intel-style bus protocol.

12. The method as recited in Claim 8 wherein said control lines are selected from the group consisting of:

an address latch enable control line,

a chip select control line,

a read control line,

a write control line,

a ready control line,

a read/write control line,

a data strobe control line, and

a data acknowledge control line.

13. The method as recited in Claim 8 wherein each segment of said address space is four kilobytes.

14. The method as recited in Claim 8 wherein said address space is a peripheral component interconnect (PCI) address space of thirty-two kilobytes.

15. A system interface processor, comprising:

a protocol data unit (PDU) receiver that receives PDUs;

a protocol data unit (PDU) transmitter that transmits PDUs; and

a peripheral component interconnect (PCI) interface that receives PDUs from said PDU receiver, transmits PDUs to said PDU transmitter and interfaces with a multi-protocol bus, said PCI interface including a multi-protocol bus system, having:

a plurality of protocol indicators associated with an address space, each of said plurality of protocol indicators associated with a segment of said address space and indicate a particular bus protocol; and

a bus protocol selection subsystem that employs control lines to implement one of said particular bus protocols in accordance with a selected one of said protocol indicators based upon an addressed segment of said address space.

16. The system interface processor as recited in Claim 15 wherein said multi-protocol bus system further includes a chip selection subsystem that provides a chip selection signal to an external device based upon said addressed segment of said address space.

17. The system interface processor as recited in Claim 16 wherein said external device is selected from the group consisting of:

a fast pattern processor,

a routing switch processor,

a Motorola-style bus architecture device, and

an Intel-style bus architecture device.

18. The system interface processor as recited in Claim 15 wherein said particular bus protocol is selected from the group consisting of:

a Motorola-style bus protocol, and

an Intel-style bus protocol.

19. The system interface processor as recited in Claim 15 wherein said control lines are selected from the group consisting of:

an address latch enable control line,

a chip select control line,

a read control line,

a write control line,

a ready control line,

a read/write control line,

a data strobe control line, and

a data acknowledge control line.

20. The system interface processor as recited in Claim 15 wherein each segment of said address space is four kilobytes.

21. The system interface processor as recited in Claim 15 wherein said address space is a peripheral component interconnect (PCI) address space of thirty-two kilobytes.